In The Claims:

Claims 1-29 (canceled)

30. (currently amended) A chip package structure comprising:

a ~~silicon~~ substrate having a surface;

a plurality of dies, wherein each die has an active surface, a backside that is opposite to the active surface, and a plurality of metal pads located on the active surface, whereas the backside of each die is adhered to the surface of the ~~silicon~~ substrate; ~~and~~

a thin-film circuit layer located over ~~on top~~ of the ~~silicon~~ substrate and the die and ~~has~~ having an external circuitry, wherein the external circuitry is electrically connected to the metal pads of the die and extends to a region outside the active surface of the die, the external circuitry has a plurality of bonding pads located on a surface layer of the thin-film circuit layer and each bonding pad is electrically connected to a corresponding metal pad of the die~~.~~:and

at least one passive device positioned inside or on the thin-film circuit layer, wherein the passive device is selected from a group consisting of an inductor, a wave-guide, a filter, and a micro electronic mechanical sensor (MEMS).

31. (original) The structure in claim 30, wherein the dies perform same functions.

32. (original) The structure in claim 30, wherein the dies perform different functions.

33. (original) The structure in claim 30, wherein the dies have an internal circuitry and a plurality of active devices located on the active surface of the die, and the internal circuitry is electrically connected to the active devices, whereas the internal circuitry forms the metal pads.

34. (currently amended) The structure in claim 33, wherein a signal from one of the active devices is transmitted to the external circuitry via the internal circuitry, and from the external circuitry back to other one of the active devices via the internal circuitry.

35. (currently amended) The structure in claim 34, wherein a width, length, ~~and~~ or thickness of the traces of the external circuitry ~~are~~ is greater than that of ~~corresponding~~ the traces of the internal circuitry.

36. (original) The structure in claim 30, wherein the external circuitry further comprising a power/ground bus.

37. (currently amended) The structure in claim 30, wherein the thin-film circuit layer comprising at least a patterned wiring layer and a dielectric layer, the dielectric layer is located ~~on top of~~ over the ~~silicon~~ substrate and the die, and the patterned wiring layer is located ~~on top of~~ over the dielectric layer, whereas the patterned wiring layer is electrically connected to the metal pads of the die through the dielectric layer and forms the external circuitry and the bonding pads of the external circuitry.

38. (currently amended) The structure in claim 37, wherein the dielectric layer has a plurality of thru-holes, and the patterned wiring layer is electrically connected to the metal pads of the die ~~by~~ via the thru-holes.

39. (currently amended) The structure in claim 38, wherein a via metal is located inside each thru-hole, and the patterned wiring layer is electrically connected to the metal pads of the die ~~by~~ via the ~~vias~~via metal.

40. (currently amended) The structure in claim 39, wherein the patterned wiring layer and the ~~vias~~ via metal form the external circuitry.

Claims 41 and 42 (canceled)

43. (currently amended) The structure in claim ~~41~~30, wherein the passive device is formed, partly or wholely, by a part of the patterned wiring layer.

44. (original) The structure in claim 37, wherein a material of the dielectric layer is selected from a group consisting of polyimide, benzocyclobutene, porous dielectric material, and stress buffer material.

45. (currently amended) The structure in claim 30, wherein the thin-film circuit layer comprising a plurality of patterned wiring layers and a plurality of dielectric layers, in which the patterned wiring layers and dielectric layers are alternately formed and the patterned wiring layers are electrically connected to the neighboring patterned wiring layers through the dielectric layer, one of the dielectric layers is

formed between the thin-film circuit layer and the ~~silicon~~ substrate, the patterned wiring layer that is closest to the ~~silicon~~ substrate is electrically connected to the metal pads of the dies through the dielectric layer that is closest to the ~~silicon~~ substrate, where the patterned wiring layer that is furthest away from the ~~silicon~~ substrate ~~forms~~ contains the bonding pads.

46. (currently amended) The structure in claim 45, wherein each of the dielectric layers has a plurality of thru-holes, by which each of the patterned wiring layer is electrically connected the neighboring patterned wiring layers, where the patterned wiring layer that is closest to the silicon substrate is electrically connected to the metal pads of the dies through the ~~dielectric layer~~ thru-holes that are closest to the substrate.

47. (currently amended) The structure in claim 46, wherein a via metal is located in each thru-hole, by which the patterned wiring layers are electrically connected to the neighboring patterned wiring layers, where the patterned wiring layer that is closest to the ~~silicon~~ substrate is electrically connected to the metal pads of the die ~~by~~ via the via metal ~~vias~~ that is closest to the substrate.

48. (currently amended) The structure in claim 47, wherein the patterned wiring layers and the ~~vias~~ via metal form the external circuitry.

Claims 49-51 (canceled)

52. (original) The structure in claim 45, wherein a material of the dielectric layer is selected from a group consisting of polyimide, benzocyclobutene, porous dielectric material, and stress buffer material.

Claim 53 (canceled)

54. (currently amended) The structure in claim 30, wherein the ~~silicon~~ substrate comprising a silicon layer and a heat conducting layer formed ~~thereon together~~overlapping, ~~a top~~ the surface of the ~~silicon~~ substrate is provided by a ~~side~~ surface of the heat conducting layer, ~~that~~ which is ~~further away from~~closer to the silicon layer, and the silicon layer has a plurality of openings that penetrate through the silicon layer ~~used~~ and is meant to form the inwardly protruded areas, ~~and the backside of~~ allowing the dies ~~is adhered to a bottom of~~ put into the inwardly protruded areas.

55. (currently amended) The structure in claim 54, wherein a thickness of the silicon ~~substrate~~ layer is approximately equal to a thickness of the dies.

56. (currently amended) The structure in claim 30 further comprising a filling layer located between ~~a~~ the surface of the ~~silicon~~ substrate and the thin-film circuit layer and surrounding the peripheral of the die, and a surface of the filling layer is planar to the active surface of the die.

57. (original) The structure in claim 56, wherein a material of the filling layer is selected from a group consisting of epoxy and polymer.

58. (original) The structure in claim 30 further comprising a passivation layer located on top of the thin-film circuit layer and exposing the bonding pads.

59. (original) The structure in claim 30 further comprising a plurality of bonding points located on the bonding pads.

60. (currently amended) The structure in claim 59, wherein the bonding points are ~~selected from a group consisting of~~ solder balls~~, bumps, and pins~~.

Claims 61-138 (canceled)

139. (new) The structure in claim 30, wherein the substrate further comprises a plurality of inwardly protruded areas located on the surface of the substrate, allowing the dies put into the inwardly protruded areas.

140. (new) The structure in claim 30, wherein the substrate is made of silicon.

Respectfully submitted,

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